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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,671	04/23/2001	Katsuaki Matsui	32011-171408	1009

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EXAMINER	
WEST, JEFFREY R	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,671	MATSUI, KATSUAKI	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-23 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-23 and 43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The Examiner does point out that Applicant's priority document contains six figures and a corresponding description of Figure 6 as conventional in the art. The instant application, however, does not contain a Figure 6 or the corresponding description (See JP Publication No. 2002-033455 and the corresponding translation provided).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 43 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 43 recites, "a length of said first wiring that connects said fourth path with said output terminal of said first selector is substantially the same as a length of said second wiring that connects said third pad with said output terminal of said second selector."

The term "substantially" in claim 43 renders the claim indefinite because the criteria for interpreting claim language is the meaning of words as they would be

understood by persons in the field of the invention. One having ordinary skill in the art would recognize that, due to the high speeds of the communication in the instant invention, differences in wiring lengths have miniscule effects on such speed. Therefore, in terms of the effect the length of the wirings have on speed/delay, substantially equal in length could encompass a wide range of differences in length, and one having ordinary skill in the art would not understood what it means to have two wiring lengths that are "substantially" the same.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21-23 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Publication No. 2000-030492 to Kurihara in view of U.S. Patent No. 5,661,685 to Lee et al. and further in view of U.S. Patent No. 5,337,321 to Ozaki.

Kurihara discloses a semiconductor device having an access time measuring test mode comprising a circuit block to which an input signal is input at a timing in accordance with an input clock, and which outputs an output signal having a value corresponding to said input signal (0001 and Figures 1 and 2), a first signal path for guiding a test input signal, which has been supplied to a first terminal, from said first

terminal to a signal input terminal of said circuit block ("ADO" in Figure 1), a second signal path for guiding a test clock, which has been supplied to a second terminal, from said second terminal to a clock input terminal of said circuit block ("CLK" in Figure 1), a third signal path for guiding a test output signal, which has been output from a signal output terminal of said circuit block, from said signal output terminal to a third terminal ("DO" through "2" and "TDO" in Figure 1), a fourth signal path for guiding said test clock, which is input to said clock input terminal, from said clock input terminal to a fourth terminal ("CLK" through "3" and "4" and "TCK" in Figure 1), wherein said third and fourth signal paths are formed so that wiring delay time of said third and fourth signal paths are substantially equal (i.e. the delay of flop-flop circuit "2" is controlled to be the same as the amount of delay in the delay circuit "4") (0014).

As noted above Kurihara teaches many of the features of the claimed invention, and while the invention of Kurihara illustrates inputting and outputting the signals at terminals/test points, Kurihara does not specify that these terminals/test points be pads.

Lee teaches a programmable logic device with a configurable power supply including means for accessing signals at a pad (column 9, line 63 to column 10, line 3).

It would have been obvious to one having ordinary skill in the art to modify the invention of Kurihara to include specifying that the terminals/test points be pads, as taught by Lee, because Kurihara does provide specific terminals/test points to allow

easy access to desired signals and Lee suggests that the combination would have provided a convenient test point to allow such access (column 9, line 63 to column 10, line 3).

As noted above, the invention of Kurihara and Lee teaches many of the features of the claimed invention and while the combination does provide means for testing a circuit block by providing specific input paths to the device and providing specific output paths to measuring pads, the combination does not specifically teach the inclusion of selectors on each of the signal paths.

Ozaki teaches a scan path circuit including means for testing a circuit block including a first signal path for guiding a test input signal to a signal input terminal of the circuit block (input to "D" of circuit block "22", Figure 2), a second signal path for guiding a test clock to a clock input terminal of the circuit block ("37", Figure 2), a third signal path for guiding a test output signal from a signal output terminal of the circuit block ("33", Figure 2), and a fourth signal path for guiding the test clock from the clock input terminal (path from branch of "37" to selector "27", Figure 2).

Ozaki also teaches that said fourth signal path has provided therein a first selector ("27", Figure 2), responsive to a mode of a selection signal (column 3, lines 9-14), that selectively supplies a prescribed signal or said test clock directly to a neighboring device (column 3, lines 15-27), wherein an output terminal of said first selector and said neighboring device are directly connected by a first wiring ("38", Figure 2).

Ozaki also teaches that said third signal path has provided therein a second selector ("26", Figure 2) which during a normal operation supplies a second prescribed signal other than said test output signal to a neighboring device and which during a test operation supplies said test output signal to said neighboring device (column 3, lines 2-14) and wherein an output terminal of said second selector and said neighboring device are directly connected by a second wiring (input to "D" of circuit block "23", Figure 2).

Ozaki also teaches that the first signal path has provided therein a third selector ("25", Figure 2) which during the normal operation supplies an output signal from a preceding circuit block to said test signal input terminal of said circuit block and which during the test operation supplies said test input signal to said signal input terminal of said circuit block (column 3, lines 2-14). Ozaki also teaches that said second signal path has provided therein a third/fourth selector ("28", Figure 2) which during the normal operation supplies a normal clock to said clock input terminal of said circuit block and which during the test operation supplies said test clock to said clock input terminal of said circuit block (column 3, lines 15-27).

It would have been obvious to one having ordinary skill in the art to modify the invention of Kurihara and Lee to specifically teach the inclusion of selectors on each of the signal paths, as taught by Ozaki, because, as suggested by Ozaki, the combination would have provided a configuration allowing the testing of the individual circuit blocks (column 1, lines 12-22), as required by the invention of Kurihara and Lee, while still allowing the normal operation of the devices, thereby

provided means for testing the individual circuit blocks in their operational environment, eliminating the burden of disconnecting the devices in order to perform testing (column 1, line 64 to column 2, line 16).

Further, while the invention of Ozaki teaches that the first and second selectors, of the third and fourth signal paths, supplies signals to neighboring devices rather than the test pads, since the invention of Kurihara and Lee teaches the outputting of the third and fourth signal paths to pads in order to measure the access time, the combination would have provided the first and second selectors, of the third and fourth signal paths, supplying signals to test pads rather than neighboring devices.

With respect to claim 43, since the specific purpose of the invention of Kurihara and Lee is to insure that the wiring delay time of said third and fourth signal paths are substantially equal and also teaches that first and second wirings connect the output of delay circuits directly with the pads wherein the first and second wiring have substantially the same length (Kurihara, Figure 1), the addition of the selectors of Ozaki would have maintained the substantially equal wiring lengths from the outputs of the selectors to the pads. Further, this would have been obvious to one having ordinary skill in the art since the invention of Kurihara and Lee requires that the delay time of said third and fourth signal paths are substantially equal, through use of delay circuits, and one having ordinary skill in the art would avoid adding a mismatch in delay times of the paths caused by implementing different wiring lengths.

Response to Arguments

6. Applicant's arguments with respect to claims 21-23 and 43 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,393,592 to Peeters et al. discloses scan flop circuitry and methods for making the same comprising a circuit block for connection to previous circuit blocks in a scan chain (column 4, lines 20-24) including a circuit block in which an input signal is input at a timing in accordance with an input clock and which outputs an output signal having a value corresponding to said input signal comprising a first signal path for guiding a test input signal to a signal input terminal of the circuit block, a second signal path for guiding a clock to a clock input terminal of the circuit block, and a third signal path for guiding an output signal (Figure 3). Peeters also discloses a selector on the first signal path which, during normal operation, supplies an output signal from a preceding circuit block to the input terminal of the circuit block and which during a test operation supplies the test input signal to the signal input terminal of the circuit block as well as a selector on the second signal path which, during normal operation supplies a normal clock to the input terminal of the circuit black and during a test operation supplies a test clock to the clock input terminal of the circuit block (Figure 3 and column 4, lines 21-39).

Peeters also discloses the conventional method of receiving and outputting the signals via test pads (Figure 1B, "SI", "CLK", and "SO").

U.S. Patent No. 6,615,380 to Kapur et al. teaches dynamic scan chains and test pattern generation methodologies comprising a plurality of circuit blocks connected in a scan chain wherein the path for guiding the test output signal from a signal output terminal includes a selector which supplies a test signal during testing and a normal output during normal operation (Figure 4 and column 2, lines 24-33).

U.S. Patent Application Publication No. 2002/0015506 to Aceti et al. teaches a remote programming and control means for a hearing aid wherein test points on a circuit board at an output stage of an amplifier are optionally connected to electrically conductive component test pads so that the sensed signal can be measured at a component tester.

U.S. Patent No. 6,578,166 to Williams teaches means for restricting the damaging effects of software faults on test and configuration circuitry including a first selector, for selecting between normal and test inputs, and a second selector, for selecting between and normal and test clock inputs.

U.S. Patent Application Publication No. 2003/0048142 to Albean teaches a controllable and testable oscillator apparatus for an integrated circuit including means for providing an output to pads and through a multiplexer.

Oracle® ThinkQuest, "Circuit Schematic Symbols" teaches the schematic symbol for a test point.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw

January 21, 2005

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800